CLAIMS

Please amend the claims as follows:

1. (previously presented) A communication link for use in a data processing system, comprising:

a receive interface to receive and convert the voltage levels of a test signal transmitted over a communication channel, where the test signal carries a clock signal and a test data signal;

a clock/data recovery (CDR) circuit coupled to the receive interface and enabled to extract the clock signal and the test data signal from the received signal; and

a debug unit configured to determine a bit error rate (BER) of the test data signal and further configured to determine at least one jitter characteristic of the communication link, wherein the debug unit further includes a test advisor configured to output a recommendation regarding a communication problem, based on the BER and the at least one jitter characteristic.

2. (original) The communication link of claim 1, further comprising a transmitter including a transmit interface connected to the communication channel and a pattern generator, wherein the transmit interface is connectable to the pattern generator.

3. (original) The communication link of claim 1, wherein the receive interface is configured to convert non-return to zero (NRZ) formatted serial data to parallel CMOS data.

4. (previously presented) The communication link of claim 1, wherein the recommendation of the test advisor indicates at least one additional test to be performed when the BER exceeds a predetermined threshold and each of the at least one jitter characteristics is acceptable.

5. (original) The communication link of claim 4, wherein the at least one additional test includes the use of a jitter tolerance pattern.

6. (previously presented) The communication link of claim 1, wherein the recommendation of the test advisor indicates a modification to a characteristic of the CDR circuit to be made when the BER

exceeds a predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold.

7. (previously presented) The communication link of claim 6, wherein:

said at least one jitter characteristic includes a high frequency jitter of the communication link; and

said modification to the CDR circuit comprises a modification to a rate of sampling the transmitted signal by the CDR circuit when the high frequency jitter of the communication link exceeds the specified threshold.

8. (previously presented) The communication link of claim 6, wherein:

said at least one jitter characteristic includes a frequency offset of the communication link; and

said modification to the CDR circuit comprises modification to a bandwidth of the CDR circuit when the frequency offset of the communication link exceeds the specified threshold.

9. (previously presented) The communication link of claim 1, wherein the CDR circuit includes an edge detector and a phase rotator control unit that is coupled to the debug unit, wherein the phase rotator control unit provides to the debug unit a signal indicative of a frequency offset of the communication link.

10. (previously presented) The communication link of claim 1, wherein the test advisor comprises a look up table (LUT) containing a plurality of entries, each entry having an associated BER value, at least one jitter characteristic value, and one of a plurality of recommendations.

11. (previously presented) A data processing system, comprising:

a first device connected to a communication channel, the first device including a communication link having a pattern generator and a transmit interface to convert a test pattern generated by the pattern generator to a test data signal for transmission via the communication channel;

a second device connected to the communication channel, the second device including a communication link receiver, comprising:

a receive interface to receive and convert the voltage levels of the test data signal transmitted over a communication channel, where the test data signal carries a clock signal and a test data signal;

a clock/data recovery (CDR) circuit coupled to the receive interface and enabled to extract the clock signal and the test data signal from the received signal; and

a debug unit configured to determine a bit error rate (BER) of the test data signal and further configured to determine at least one jitter characteristic of the communication link, wherein the debug unit further includes a test advisor configured to recommend, based on the BER and the at least one jitter characteristic, corrective action responsive to the BER exceeding a predetermined threshold.

12. (previously presented) The system of claim 11, wherein the corrective action recommended by the test advisor includes performing at least one additional test when the BER exceeds the predetermined threshold and each of the at least one jitter characteristics is acceptable.

13. (previously presented) The system of claim 11, wherein the corrective action recommended by the test advisor includes modifying a characteristic of the CDR circuit when the BER exceeds the predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold.

14. (previously presented) The system of claim 13, wherein said corrective action includes modifying a rate of sampling the transmitted signal by the CDR circuit when the at least one jitter statistic that exceeds the specified threshold is a statistic indicative of high frequency jitter of the communication link.

15. (previously presented) The system of claim 13, wherein said correction action includes modifying a bandwidth of the CDR circuit when the at least one jitter statistic that exceeds the specified threshold is a statistic indicative of a frequency offset of the communication link.

16. (previously presented) The system of claim 11, wherein the CDR circuit includes an edge detector and a phase rotator control unit that are each coupled to the debug unit, wherein the edge detector provides to the debug unit a signal indicative of high frequency jitter of the communication link and the phase rotator control unit provides to the debug unit a signal indicative of a frequency offset of the communication link.

17. (previously presented) The system of claim 11, wherein the test advisor comprises a look up table (LUT) containing a plurality of entries, each entry having an associated BER value, at least one jitter characteristic value, and one of a plurality of recommendations.

18. (previously presented) An integrated circuit, comprising:

a transceiver including a receive interface suitable for connecting the integrated circuit to a serial communication channel;

a clock/data recovery (CDR) circuit connected to the receive interface and configured to extract a clock signal and a test data signal from a signal received via the communication channel;

a debug unit including:

means for determining a bit error rate (BER) of the test data signal;

means for determining at least one jitter characteristic of the communication link; and

means for using the BER and the at least one jitter characteristic to generate an action recommendation if the BER exceeds a specified threshold.

19. (original) The integrated circuit of claim 18, wherein the debug unit includes means for determining high frequency jitter magnitude and frequency offset of the communication link.

20. (original) The integrated circuit of claim 19, wherein the means for generating an action recommendation includes means for accessing a look up table (LUT) to retrieve the action recommendation based on the BER, the high frequency jitter margin and the frequency offset.